CLAIMS:

1. A packet processor, comprising: a plurality of logic blocks, including a first logic block for performing one or more processing operations on packet data and a second logic block for performing one or more processing operations on packet data in response to packet data output from said first logic block, wherein at least one of said first or second logic blocks outputs packet data in response to packet data input at time T + t, wherein t > 0, to said at least one logic block prior to outputting packet data in response to packet data input at time T to said at least one logic block.

2. The packet processor of claim 1, wherein said at least one of said first or second logic blocks alternates between processing said packet data input at time T + t and said packet data input at time T.

3. A packet processor, comprising: a plurality of logic blocks, including a first logic block for performing one or more processing operations on packet data and a second logic block for performing one or more processing operations on packet data in response to packet data output from said first logic block, wherein at least one of said first or second logic blocks accepts packet data at time T + t, wherein t > 0, prior to outputting packet data accepted at time T.

4. The packet processor of claim 3 wherein said at least one of said first or second logic blocks alternates between processing said packet data accepted at time T + t and said packet data accepted at time T.

5. A packet processor including a plurality of logic blocks, each logic block comprising:

an input receiving a first packet data associated with a first packet at time T and a second packet data associated with a second packet at time T + t, wherein t > 0;

a storage device storing the first packet data and the second packet data;

a sub-processor coupled to the storage device, the sub-processor alternating between processing the first packet data and the second packet data and outputting to a next logic block the second packet data prior to outputting the first packet data.

6. The packet processor of claim 5, wherein the input receives a third packet data associated with a third packet at time T + t', wherein t' > t, prior to outputting the first or second packet data.

7. A packet processor including a plurality of logic blocks, each logic block comprising:

an input receiving a first packet data associated with a first packet and a second packet data associated with a second packet;

a storage device storing the first packet data and the second packet data;

a sub-processor coupled to the storage device, the sub-processor switching from processing the first packet data to

processing the second packet data while awaiting a processing result for the first packet data.

8. The packet processor of claim 7, wherein the processing result is a conditional branch instruction result.

9. A pipelined processor comprising a plurality of logic blocks, a first logic block for performing a first operation on a first processing instruction associated with a first packet and forwarding the first processing instruction to a second logic block for performing a second operation, the first logic block receiving a second processing instruction associated with a second packet if a potential stall is expected in processing the first processing instruction, the first logic block performing the first operation on the second processing instruction concurrently with the second operation on the first processing instruction.

10. The pipelined processor of claim 9, characterized in that the first logic block receives a third processing instruction associated with the first packet if no potential stall is expected in processing the first processing instruction.

11. The pipelined processor of claim 9, wherein the potential stall is created by a conditional branch instruction.

12. A method for processing packets in a packet processor including a first logic block for performing one or more processing operations on packet data and a second logic block

for performing one or more processing operations on packet data in response to packet data output from said first logic block, the method comprising the steps of:

receiving by the first logic block at time T a first packet data;

processing the first packet data;

receiving by the first logic block at time T + t, wherein t > 0, a second packet data;

processing the second packet data; and

outputting a third packet data to the second logic block in response to the second packet data input at time T + t prior to outputting a fourth packet data to the second logic block in response to the first packet data input at time T.

13. The method of claim 12 further comprising the step of alternating between processing the second packet data input at time T + t and the first packet data input at time T.

14. A method for processing packets in a packet processor including a first logic block operative for performing one or more processing operations on packet data and a second logic block for performing one or more processing operations on packet data in response to packet data output from said first logic block, the method comprising the steps of:

receiving by the first logic block at time T a first packet data;

outputting the first packet data to the second logic block; and

receiving by the first logic block at time T + t, wherein t > 0, a second packet data prior to outputting to the second logic block the first packet data received at time T.

15. The method of claim 14 further comprising the step of alternating between processing the second packet data received at time T + t and the first packet data received at time T.

16. A method for processing packets in a packet processor including a first logic block and a second logic block, the method comprising the steps of:

receiving at the first logic block at time T a first packet data associated with a first packet;

receiving at the first logic block at time T + t, wherein t > 0, a second packet data associated with a second packet;

alternating between processing the first packet data and the second packet data; and

outputting to the second logic block the second packet data prior to outputting the first packet data.

17. The method of claim 16 further comprising the step of receiving a third packet data associated with a third packet at time T + t', wherein t' > t, prior to outputting the first or second packet data.

18. A method for processing packets in a packet processor including a first logic block and a second logic block, the method comprising the steps of:

receiving at the first logic block a first packet data associated with a first packet and;

receiving at the first logic block a second packet data associated with a second packet;

processing the first packet data; and

switching from processing the first packet data to processing the second packet data while awaiting a processing result for the first packet data.

19. The method of claim 18, wherein the processing result is a conditional branch instruction result.

20. A method for processing packets in a pipelined processor having a plurality of logic blocks, the method comprising the steps of:

performing at the first logic block a first operation on a first processing instruction associated with a first packet;

forwarding the first processing instruction to a second logic block for performing a second operation; and

receiving at the first logic block a second processing instruction associated with a second packet if a potential stall is expected in processing the first processing instruction, the first logic block performing the first operation on the second processing instruction concurrently with the second operation on the first processing instruction.

21. The method of claim 20 further comprising the step of receiving at the first logic block a third processing instruction associated with the first packet if no potential stall is expected in processing the first processing instruction.

22. The method of claim 20, wherein the potential stall is created by a conditional branch instruction.